REMARKS

In the Official Action mailed on **28 November 2005**, the Examiner reviewed claims 1-27. Claims 1-6, 10-19, and 23-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Rajwar et al (*Speculative Lock Elision*; ACM/IEEE International Symposium; Dec. 2001, hereinafter "Rajwar"), and further in view of Jim Gray (*The Transaction Concept: Virtues and Limitations*, hereinafter "Gray") and Microsoft Computer Dictionary (Fifth edition, published in 2002, hereinafter "MCD"). Claims 7-9 and 20-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Rajwar, in view of Gray, in view of MCD and further in view of Gaskins et al (USPN 6,681,311, hereinafter "Gaskins").

Rejections under 35 U.S.C. §103(a)

Independent claims 1, 14, and 27 were rejected as being unpatentable over Rajwar and further in view of Gray and MCD. Applicant respectfully points out that the combined system of Rajwar, Gray, and MCD teaches speculatively eliding locks for critical sections of code **without hardware support** by using a filter, and then determining if there were conflicts within the critical section of code (see Rajwar, Abstract, paragraph 1, and page 298, col. 1, lines 1-2).

In contrast, the present invention provides **hardware support for transactional execution** of critical sections of code. More specifically, the present invention provides hardware to support a "start transactional execution" instruction and a "commit" instruction (see FIG. 2, and paragraphs [0057]-[0060] of the instant application). This is beneficial because it provides the ability to selectively monitor specific load and store instructions within the critical sections of code, while not monitoring other load and store instructions that cannot interfere with the architectural state of the machine. There is nothing within Rajwar, Gray, or MCD, either separately or in concert, which suggests providing

hardware support for transactional execution of critical sections of code, wherein the transactional execution involves executing a "start transactional execution" instruction and a "commit" instruction. In fact, Rajwar teaches away from the present invention because no hardware support is provided.
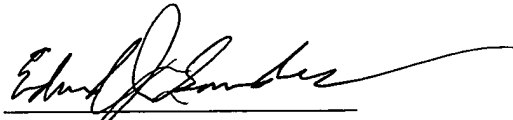
Accordingly, Applicant has amended independent claims 1, 14, and 27 to clarify that the present invention provides hardware support for transactional execution of critical sections of code, wherein the transactional execution involves executing a hardware-supported "start transactional execution" instruction and a "commit" instruction. These amendments find support in FIG. 2, and in paragraphs [0057]-[0060] of the instant application.

Hence, Applicant respectfully submits that independent claims 1, 14, and 27 as presently amended are in condition for allowance. Applicant also submits that claims 2-13, which depend upon claim 1, and claims 15-26, which depend upon claim 14, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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